

2



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
 Address: COMMISSIONER FOR PATENTS  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
 www.uspto.gov

6

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,019	12/18/2001	Andrew Mark Player	applied_106	2473

7590 10/05/2004  
 Law Office of Gerald Maliszewski  
 P.O. Box 270829  
 San Diego, CA 92198-2829

EXAMINER

SURYAWANSHI, SURESH

ART UNIT PAPER NUMBER

2115

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

6

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/023,019		PLAYER, ANDREW MARK	
	<b>Examiner</b>		<b>Art Unit</b>	
	Suresh K Suryawanshi		2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 18 December 2001.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 December 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 12/18/01.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. Claims 1-33 are presented for examination.

#### ***Drawings***

2. This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claim limitation of the claim 31 "... at least one locking register includes a plurality of locking registers ..." must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must

Art Unit: 2115

be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

#### ***Claim Objections***

4. Claim 22 is objected to because of the following informalities: word "in" should have been "is" in the phrase "wherein the device in configured in response" at page 20, line 8. Appropriate correction is required.

#### ***Specification***

5. The abstract of the disclosure is objected to because it contains more than 150 words. Correction is required. See MPEP § 608.01(b).

Art Unit: 2115

***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 31 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 31 claims that at least one locking register includes a plurality of locking registers. Examiner was unable to find a supportive detail in the provided specification or locate in the provided drawings.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by MacDonald et al (US Patent no 6,557,101 B1).

Art Unit: 2115

10. As per claim 1, MacDonald et al disclose in a network-connected integrated circuit device, a method for securely provisioning configuration data [fig. 2], the method comprising:

receiving configuration data [fig. 2; col. 3, lines 34-65; col. 4, lines 9-23; the control logic 12' receives data from the microprocessor 14];

loading the configuration data [fig. 2; col. 3, lines 34-65; col. 4, lines 9-23; the control logic 12' loads data into the latches 20]; and

locking to prevent the loading of subsequently received configuration data [fig. 2; col. 3, lines 34-65; col. 4, lines 9-23; immediate prior to the re-programming, the control logic 12' toggles the latch enable signal to close the latches 20].

11. As per claim 14, MacDonald et al disclose in a system of networked devices, a method for securely provisioning configuration data [fig. 2], the method comprising:

booting the system up [booting is inherent to bring the system up];

supplying data to provision at least one network-connected device [fig. 2; col. 3, lines 34-65; col. 4, lines 9-23; the control logic 12' supplies data to device(s) 10 through the latches 20];  
and

locking the network-connected device to prevent subsequent data provisioning [fig. 2; col. 3, lines 34-65; col. 4, lines 9-23; immediate prior to the re-programming, the control logic 12' toggles the latch enable signal to close the latches 20 and therefore preventing subsequent data provisioning].

***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 2-13 and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacDonald et al (US Patent no 6,557,101 B1) in view of Cline et al (US Patent no 4,665,506).

14. As per claims 2 and 15, MacDonald et al disclose the invention substantially. MacDonald et al do not expressly disclose about configuration registers. However, configuration registers are well known in the art as expressly disclosed by Cline et al [col. 7, lines 21-23, 32-33; the configuration register 8]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to provide protection against unwanted overwrites. Moreover, the use of a configuration register will provide a simple and faster read/write circuitry.

15. As per claims 3-4 and 16-17, MacDonald et al disclose the invention substantially.

MacDonald et al do not disclose about a locking register that is used to prevent loading of data in a configuration register. However, Cline et al clearly disclose about such a register to write protect the configuration register [col. 7, lines 21-23, 32-33, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to provide protection against unwanted overwrites.

16. As per claims 5 and 18, MacDonald et al disclose the invention substantially.

MacDonald et al do not disclose about a locking register that is used to prevent loading of data in a configuration register. However, Cline et al clearly disclose about such a register to write protect the configuration register. Clearly, the protection register has to be loaded with a lock set to indicate that the configuration register is write protected. Similarly it will be loaded with a non-lock set to enable the write operation [col. 7, lines 21-23, 32-34, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to provide protection against unwanted overwrites.



17. As per claims 6 and 19, MacDonald et al disclose the invention substantially. MacDonald et al do not disclose about a locking register. However, Cline et al clearly disclose about a locking register to indicate if the configuration register is write protected. This write protect register is an 8-bit register. Clearly, the protection register has to be loaded with a non-lock set to indicate that the configuration register is not write protected. Similarly, it will be loaded with a lock set (different than the non-lock set) to indicate that the configuration register is write protected [col. 7, lines 21-23, 32-34, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to provide protection against unwanted overwrites.

18. As per claim 7, MacDonald et al disclose the invention substantially. MacDonald et al do not disclose about having two locking registers. However, Cline et al clearly disclose about the write protection registers 10 and 11 and loading a first lock set in the first locking register and a second lock set in the second locking register is inherent [col. 7, lines 21-23, 32-34, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to provide protection against unwanted overwrites.

19. As per claim 8, MacDonald et al disclose the invention substantially. MacDonald et al do not disclose about having a first locking register and a second locking registers. However, Cline et al clearly disclose about the write protection registers 10 and 11 and each register will have it's own address [col. 7, lines 21-23, 32-34, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to provide protection against unwanted overwrites.

20. As per claims 9 and 10, MacDonald et al disclose the invention substantially. MacDonald et al do not disclose about having a first and a second locking registers. However, Cline et al clearly disclose about the write protection registers 10 and 11 [col. 7, lines 21-23, 32-34, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8]. These 8-bit registers 10 and 11 could have same lock sets values or different lock set values because both are used to write protect the configuration register 8 from CPU and DMA. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to provide protection against unwanted overwrites.

21. As per claim 11, MacDonald et al disclose the invention substantially. MacDonald et al do not disclose about having a plurality of locking registers. However, Cline et al clearly disclose about having a plurality of locking registers [col. 7, lines 21-23, 32-34, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8]. These 8-bit registers will have a corresponding plurality of addresses. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to provide protection against unwanted overwrites.

22. As per claims 12 and 20, MacDonald et al disclose the invention substantially. MacDonald et al do not disclose about having a locking register. However, Cline et al clearly disclose about having a locking register and permitting write access to the configuration register in response to the non-lock set in the locking register [col. 7, lines 21-23, 32-34, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to provide protection against unwanted overwrites.

Art Unit: 2115

23. As per claims 13 and 21, MacDonald et al disclose the invention substantially.

MacDonald et al do not disclose about having a locking register. However, Cline et al clearly disclose about having a locking register and loading a non-lock set in the locking register to enable write access to the configuration register [col. 7, lines 21-23, 32-34, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8]. And inherently the non-lock set being a key set having a unique value as to distinct it from the lock set value. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to provide protection against unwanted overwrites.

24. Claims 22-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cline et al (US Patent no 4,665,506).

25. As per claim 22, Cline et al clearly disclose a configuration register and the device is configured in response to the data in the configuration register [col. 4, lines 52-54; the actual path depends upon the state of the pipeline control bit in the configuration register 8; col. 7, lines 21-23, 32-34]; and Cline et al also disclose about at least one locking register that is used to prevent the loading of data in the configuration registers [col. 7, lines 21-23, 32-34, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8].

Cline et al do not disclose about having a plurality of configuration registers in the system as in the disclosed system of Cline et al only one configuration register is required [col. 4, lines 52-54; col. 7, lines 21-23, 32-34]. However, a routineer in the art would be able to implement multiple configuration registers after the knowledge of implementation of one configuration register. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a plurality of configuration registers as needed after having the knowledge of implementation of one configuration register.

26. As per claims 23 and 24, Cline et al disclose the locking register to prevent the loading of data in the configuration register [col. 7, lines 21-23, 32-33, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8].

27. As per claim 25, Cline et al disclose about having a locking register and loading a non-lock set in the locking register to enable write access to the configuration register [col. 7, lines 21-23, 32-33, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8]. And inherently the non-lock set being a key set having a unique value as to distinct it from the lock set value.

28. As per claim 26, Cline et al disclose about having a locking register to prevent or allow loading of data into the configuration register [col. 7, lines 21-23, 32-33, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8].

Art Unit: 2115

29. As per claim 27, Cline et al disclose having two locking registers [col. 7, lines 21-23, 32-33, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8].

30. As per claim 28, Cline et al disclose that the first and second locking registers having non-contiguous first and second addresses [col. 7, lines 50-54; registers 10 and 11].

31. As per claims 29 and 30, Cline et al disclose that the first and second lock sets have values that are equal or not equal [col. 7, lines 50-54; registers 10 and 11].

32. As per claim 32, Cline et al disclose that at least one locking register accepts a non-lock set, following the loading the first lock set, and permits write access to the configuration registers in response to the non-lock set [col. 7, lines 21-23, 32-34, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8 and therefore there has to be a non-lock set and a lock set value to permit or prevent write access].

33. As per claim 33, Cline et al disclose that the non-lock set is a key set with a unique value [col. 7, lines 21-23, 32-33, 50-54; registers 10 and 11 provide protection against CPU and DMA initiated overwrites to the configuration register 8 and inherently the non-lock set being a key set having a unique value as to distinct it from the lock set value].

Art Unit: 2115

***Conclusion***

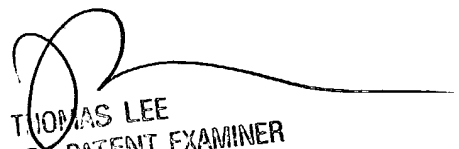
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 703-305-3990 (starting 10/18/04, please use 571-272-3668). The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717 (starting 10/18/04, please use 571-272-3667). The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks

September 21, 2004

  
THOMAS LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100